REMARKS

This is a response to the final Office Action dated September 21, 2006. Claims 1-20 were rejected.

In this paper, Claim 5 is amended. Claims 21-26 are new. Upon entry of this Amendment, Claims 1-26 will be pending. No new matter is added by way of these amendments. Furthermore, for at least the reasons discussed herein, the presently pending claims are now in condition for allowance.

Claim Rejections - 35 U.S.C. § 103

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al., U.S. Patent Publication No. 2004/0032406 ("Agarwal"), in view of Donnelly et al., U.S. Patent Publication No. 2004/0223571 ("Donnelly"), and in further view of Agazzi, U.S. Patent Publication No. 2002/0122503 ("Agazzi").

Agarwal is generally directed towards a computer program to calculate the optimal sampling phase and frequency for a video signal. (Abstract of Agarwal). The microcontroller 410 sets the output frequency for single-output PLL 416 and the phase delay for single-output DLL 406 to calculated optimal values for ADC 411-13 clocking. (Fig. 3; pg. 3, paragraph [0044-56] of Agarwal). Agarwal does not disclose or suggest a plurality of outputs for PLL 416.

Donnelly is generally directed towards the use of a DLL based system to generate an output clock with a desired phase delay. (Pg. 1, paragraph [0003] of Donnelly). Donnelly discloses that this method improves upon PLL based circuits by reducing phase error in response to PLL input changes and problems caused by PLL instability. (Pg. 1, paragraph [0004] of Donnelly). Donnelly does not disclose the use of a PLL.

Agazzi is generally directed towards a deserialization technique for high speed serial data. (Abstract of Agazzi). These techniques allow for compensation to be applied to sampling controls or sampled data.

Claim 1 is respectfully submitted to be allowable at least because (1) Agarwal, Donnelly, and Agazzi fail to disclose or suggest all elements of Claim 1 and (2) there is no motivation to combine Donnelly with Agarwal.

First, Agarwal, Donnelly, and Agazzi, either singly or in any combination, fail to disclose or suggest "a phase locked loop (PLL) circuit adapted to generate a plurality of phased signals" as recited by Claim 1. The Office Action points to fig. 4 and paragraph [0027] of Agarwal as disclosing a PLL that generates a plurality of phased signals. However, the Agarwal's PLL is only capable of generating a single output. Agarwal fails to disclose or suggest the generation of a plurality of output signals and the phasing of the pluralities of outputs. Additionally, Donnelly and Agazzi both also fail to disclose or suggest a PLL with a plurality of outputs. In fact, Donnelly specifically eschews use of PLLs due to the problems with second order stability and output errors that occur in response to inputs changes or power supply variations. (Pg. 1, paragraph [0004] of Donnelly). These problems are common to PLL circuits.

Second, there is no motivation to combine Donnelly with Agarwal. As discussed above, Donnelly specifically teaches away from the use of PLLs. As such, Donnelly teaches use of a DLL rather than a PLL – not the combination of a PLL with a DLL. Therefore, one of ordinary skill in the art would not be motivated to combine Donnelly with Agarwal.

Accordingly, Claim 1 is allowable for at least the above reasons.

In addition to the reasons above regarding Claim 1, upon which Claim 5 depends, Claim 5 also is respectfully submitted to be allowable at least because none of the cited references either singly or in any combination disclose or suggest a circuit "wherein the first selected phased signal, the second selected phased signal, and at least one selected phase information signal are received into the phase mixer."

As can be seen in fig. 6 of Donnelly, phase interpolator 560 only receives selected phased signals Kx and Ky from the selection circuitry 510. Donnelly fails to disclose or suggest a phase mixer that receives at least one selected phase information signal in addition to first and

second selected phased signals. Likewise, Agarwal and Agazzi also fail to disclose or suggest such a phase mixer. Thus Claim 5 is allowable.

Independent Claims 11 and 13 are respectfully submitted to be allowable for at least reasons similar to those given above in respect to Claim 1.

New Claims 21-26 were added to point out what the Applicant regards as the invention and these claims are supported at least by fig. 13 and pg. 8, lines 1-3 of the specification. These new claims are respectfully submitted to be allowable for at least the reasons discussed above regarding Claims 1 and 5 upon which they depend.

Additionally, it is respectfully submitted that the remaining dependent Claims 2-4, 6-10, 12, and 14-20 are allowable at least based on their dependence on one of Claims 1, 11, or 13.

CONCLUSION

This response has addressed fully all of the concerns expressed in the instant Office Action and Claims 1-26 are in condition for allowance. Early favorable action is urged. Should any further aspects of the application remain unresolved, the Examiner is invited to telephone the Applicant's attorney at the number listed below.

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Respectfully submitted,

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